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3.3V Parallel interface transceiver/buffer PDI1284P11

FEATURES

- Asynchronous operation
- 8-Bit transceivers
- 6 additional buffer/driver lines peripheral to cable
- 5 additional control lines from cable
- 5V tolerant
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Latch up protection exceeds 500 mA per JEDEC Std 19
- Input Hysteresis
- Low Noise Operation
- IEEE 1284 Compliant Level 1 & 2
- Overvoltage Protection on B/Y side for OFF-state
- A side 3-State option
- B side active or resistive pull up option
- Cable side V_{CC} for 5V or 3V operation

DESCRIPTION

The PDI1284P11 parallel interface chip is designed to provide an asynchronous, 8-bit, bi-directional, parallel interface for personal computers. The part includes all 19 signal lines defined by the IEEE1284 interface specification for Byte, Nibble, EPP, and ECP modes. The part is designed for hosts or peripherals operating at 3.3V to interface 3.3V or 5.0V devices.

The 8 transceiver pairs (A/B 1-8) allow data transmission from the A bus to the B bus, or from the B bus to the A bus, depending on the state of the direction pin DIR.

The B bus and the Y9-Y13 lines have either totem pole or resistor pull up outputs, depending on the state of the high drive enable pin HD. The A bus has only totem pole style outputs. All inputs are TTL compatible with at least 400mV of input hysteresis at V_{CC} = 3.3V.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
R_D	B/Y Side output resistance	V_{CC} = 3.3V; V_O = 1.65V ±0.2V (See Figure 2)	45	Ω
R_{PU}	B/Y side pull up resistance	V_{CC} = 3.3V; Outputs, resistive pull up	1.4K	Ω
SR	B/Y Side slew rate	R_L = 62Ω; C_L = 50pF (See Waveform 4)	0.2	V/ns
I_{CC}	Total static current	$V_I = V_{CC}$/GND; I_O = 0	5	µA
V_{HYS}	Input hysteresis	V_{CC}= 3.3V	0.47	V
t_{PLH}/t_{PHL} A –B/Y	Propagation delay to the B/Y side outputs	V_{CC} = 3.3V	12.5/13.9	ns

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
48-pin plastic SSOP Type II	0°C to +70°C	PDI1284P11 DL	SOT370-1
48-pin plastic TSSOP Type II	0°C to +70°C	PDI1284P11 DGG	SOT362-1

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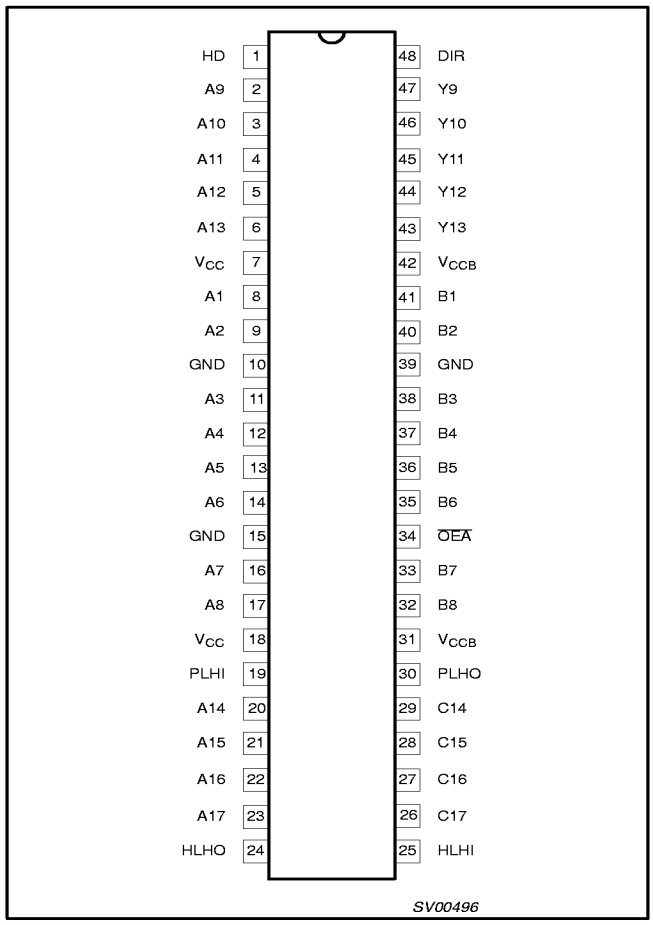
PIN CONFIGURATION



PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
8, 9, 11, 12, 13, 14, 16, 17	A1 - A8	Data inputs/outputs
41, 40, 38, 37, 36, 35, 33, 32	B1 - B8	IEEE 1284 Std. outputs/inputs
2, 3, 4, 5, 6	A9 - A13	Data inputs
47, 46, 45, 44, 43	Y9 - Y3	IEEE 1284 Std. outputs
29, 28, 27, 26	C14 - C17	Control inputs (cable)
20, 21, 22, 23	A19 - A17	Control outputs (peripheral)
1	HD	B/Y–side high drive enable/disable
48	DIR	Direction selection A to B / B to A
19	PLHI	Peripheral logic high input (peripheral)
30	PLHO	Peripheral logic high output (cable)
25	HLHI	Host logic high input (cable)
24	HLHO	Host logic high output (cable)
10, 15, 39	GND	Ground (0V)
7, 18	V_{CC}	Positive supply voltage
31, 42	V_{CCB}	Cable side power supply voltage 3V/5V
34	$\overline{OEA}$	A side output enable

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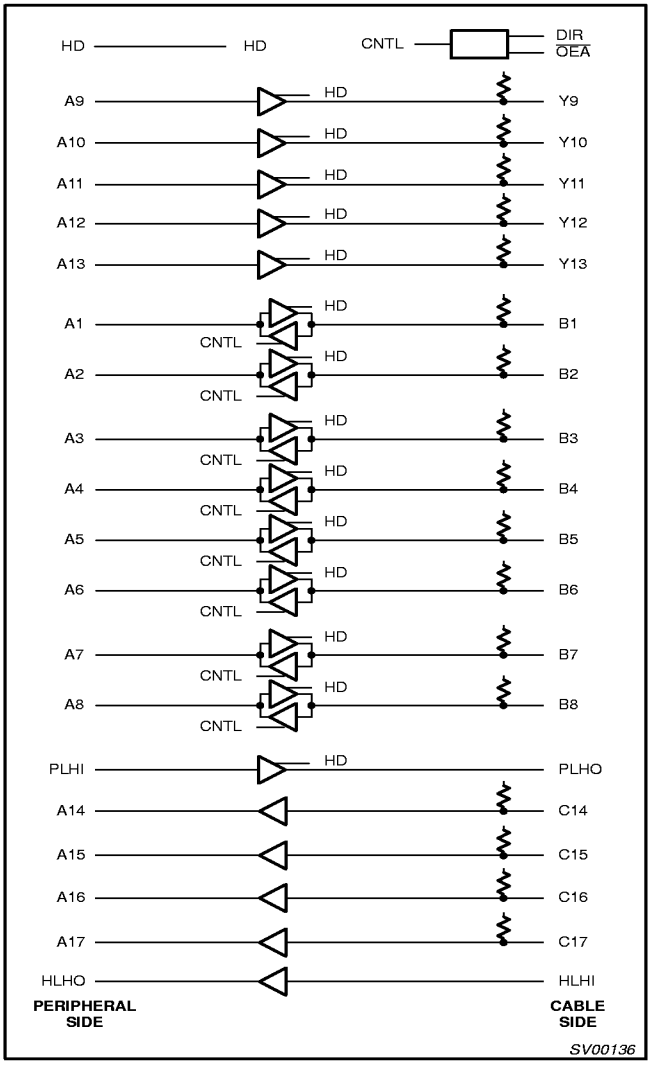
LOGIC SYMBOL



PINS WITH PULL UP RESISTORS TO LOAD CABLE

PINS	SYMBOL	FUNCTION
47, 46, 45, 44, 43	Y9 – Y13	Output cable drivers
41, 40, 38, 37, 36, 35, 33, 32	B1 – B8	Output cable drivers
29, 28, 27, 26	C14 – C17	External cables control signal input

FUNCTION TABLE

DIR	$\overline{OEA}$	HD	INPUTS	OUTPUTS	OUTPUT TYPES
X	X	X	C14-17	A14-17	t_P
X	X	X	HLHI	HLHO	t_P
X	X	L	A9-13	Y9-13	r_P
X	X	H	A9-13	Y9-13	t_P
X	X	L	PLHI	PLHO	O.C.
X	X	H	PLHI	PLHO	t_P
H	X	L	A1-8	B1-8	r_P
H	X	H	A1-8	B1-8	t_P
L	L	X	B1-8	A1-8	t_P
L	H	X		A1-8	Z*
L	H	X	B1-8		r_P*

A = Side driving internal IC
B = Side driving external cable (bidirectional)
C = Side receiving control signals from internal cable
Y = Side driving external cable (unidirectional)
X = Don't care – control signals in
Z = High Z or 3-State
O.C. = Open collector
t_P = Totem pole output
r_P = Resistive pull up: 1.4kΩ (nominal) on B/Y/C cable side and V_{CC}. However, while a B/Y side output is Low as driven by a Low signal on the A side, that particular B/Y side resistor is switched out to stop current drain from V_{CC} through it.
* When DIR = L and $\overline{OEA}$ = H, the output signal is isolated from the input signal. B1 – 8 signals maintain an r_P = 1.4kΩ on the input for this mode.

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ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
	ESD Immunity, per Mil Std 883C method 3015		± 1	kV
V_{CC}	DC supply voltage		–0.5 to +4.6	V
V_{CCB}	DC cable supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	±20	mA
I_{OK}	DC output diode current	$V_O < 0$	±50	mA
V_{IN}	DC input voltage[3]		–0.5 to +5.5	V
V_{OUT} B/Y	DC output voltage on B/Y side[3]		–0.5 to +5.5	V
V_{OUT} B/Y	Transient output voltage on B/Y side[4]	40ns transient	–2 to +7	V
V_{OUT} A	DC output voltage on A side		–0.5 to V_{CC} +0.5	V
I_O	DC output current	Outputs in High or Low state	±50	mA
T_{stg}	Storage temperature range		–60 to +150	°C
I_{CC}/I_{GND}	Continuous current through V_{CC} or GND		±200	mA

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
4. V_{OUT} B/Y (tr) guarantees only that this part will not be damaged by reflections in application so long as the voltage levels remain in the specified range.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	3.0	3.6	V
V_{CCB}	DC cable supply voltage	3.0	5.5	V
V_{IH}	High level Input voltage	2.0		V
V_{IL}	Low level input voltage		0.8	V
V_{OUT} B/Y	B/Y output voltage	–0.5	5.5	V
V_{OUT} A	A side output voltage	0	V_{CC}	V
I_{OH}	B/Y side output current High		–14	mA
I_{OL}	B/Y side output current Low		14	mA
T_{amb}	Operating free-air temperature range	0	+70	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T_{amb} = 0°C to 70°C			
			MIN	TYP	MAX	
V_{HYS}, A, B	Input hysteresis	A, B, control inputs, V_{CC} = 3.3V, V_{IL}= 0.8, V_{IH} = 2.0	0.4			V
V_{IH}, A, B, PLHI	High-level input voltage	V_{CC} = 3.0 to 3.6V	2.0			V
V_{IL}, A, B, PLHI	Low-level input voltage	V_{CC} = 3.0 to 3.6V			0.8	V
V_{HYS}, C	Input hysteresis	C Inputs, V_{CC} = 3.3V	0.8			V
V_{IH}, C	High-level input voltage	C Inputs, V_{CC} = 3.0 to 3.6V	2.3			V
V_{IL} C	Low-level input voltage	V_{CC} = 3.0 to 3.6V			0.8	V
V_{IH} HLH	High-level input voltage	V_{CC} = 3.6V	2.6			V
V_{IL} HLH	Low-level input voltage	V_{CC} = 3.0			1.55	V
RD_P	Output impedance	V_{CC} = 3.3V, V_O = 1.65 ±0.1V See Fig. 2	35	45	55	Ω
RD_N	Output impedance	V_{CC} = 3.3V, V_O = 1.65 ±0.1V See Fig. 2	35	45	55	Ω
R_{PU}	Pull up resistance	V_{CC} = 3.3V, outputs in high Z	1.15	1.4	1.65	kΩ
V_{OH}, B/Y	High-level output voltage	V_{CC} = 3.0V, I_{OH} = –14mA	2.23			V
V_{OL}, B/Y	Low-level output voltage	V_{CC} = 3.0V, I_{OL} = 14mA			0.77	V
V_{OH}, A and HLH	High-level output voltage	I_{OH} = –500µA, V_{CC} = 3.0V	2.8			V
		I_{OH} = –4mA, V_{CC} = 3.0V	2.4			
V_{OL}, A and HLH	Low-level output voltage	I_{OL} = 50µA, V_{CC} = 3.0V			0.2	V
		I_{OL} = 4mA, V_{CC} = 3.0V			0.4	
V_O PLH	High-level output voltage	I_{OH} = 500µA, V_{CC} = 3.15V	3.1			V
	Low-level output voltage	I_{OL} = 500µA, V_{CC} = 3.0V			0.8	
I_{CC}	Quiescent supply current for V_{CC} and V_{CCB} under all conditions except when B or C inputs are LOW	V_{CC} = 3.6V, V_{CCB} = 3.6V to 5.5V V_{in} = 0 or V_{CC}; V_{Bin} = V_{CCB} Vcin = V_{CCB} or Floating		0.1	100	µA
I_{CCBL}[2]	Quiescent supply current for VCCB when B or C inputs are LOW	V_{CC} = V_{CCB} = V_{dir} = 3.6V V_{in} = 0 or V_{CC}; V_{cin} = 0V		10	15	mA
		V_{CC} = V_{dir} = 3.6V; V_{CCB} = 5.5V V_{in} = 0 or V_{CC}; V_{cin} = 0V		16	20	mA
		V_{CC} = V_{CCB} = 3.6V; V_{dir} = 0V V_{in} =0 or V_{CC}; V_{Bin} = V_{cin} = 0V		30	40	
		V_{CC} = 3.6V, V_{CCB} = 5.5V; V_{dir} = 0V V_{in} = 0 or V_{CC}; V_{Bin} = V_{cin} = 0 V		47	60	
I_{off} C/B/Y side	Power off leakage current	V_O = 5.5V, V_{CC} = V_{CCB} = 0			+ 100	µA
		V_O = 5.5V, V_{CC} = 0, V_{CCB} = 4.5V			±100	
I_{in}[1]	Input leakage current	Input leakage current[1] V_{in} = 0 to V_{CC}			±1	µA
I_{OZ}[1]	3-State output current	V_{OUT} = V_{CC} or GND			±20	µA

NOTES:
1. The pull up resistor on the B side outputs makes it impossible to test I_{OZ} on the B side. This applies to the input current on the C side inputs as well.
2. Includes extra ICCB current from pull-up resistors, i.e. ICCBL = (#B + #C LOW inputs) * (VCCB/R_{PU}).

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AC CHARACTERISTICS

GND = 0V, $t_R = t_F = 3.0ns$, $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	TEST CONDITIONS	WAVEFORMS	LIMITS T_{amb} = 0°C to +70°C			UNIT
				MIN	TYP	MAX	
tp_{LH}	Propagation delay	Path A to B or Y	2, 5	0		20	ns
tp_{HL}				0		20	
tp_{LH}	Propagation delay	Path B to A	2, 5	0		12	ns
tp_{HL}				0		12	
tp_{LH}	Propagation delay	Path C to A	2, 5			15	ns
tp_{HL}						15	
tp_{LH}	Propagation delay	Path PLH	2, 5			20	ns
tp_{HL}						20	
tp_{LH}	Propagation delay	Path HLH	2, 5			15	ns
tp_{HL}						15	
t_{slew}	Slew rate	B or Y side outputs	4	0.05		0.4	V/ns
tp_{HZ}	Output enable/ disable time	HD to Y or B $R_L = 500\Omega$	3			20	ns
tp_{ZH}						20	
t_{DIFF}	Propagation delay difference	HD prop tp_{ZH}–tp_{HZ}				10	ns
tp_{HZ}	Output enable time	HD to PLHO $R_L = 500\Omega$	3			20	ns
tp_{ZH}						20	
tp_{HZ}	Output enable/ disable time	Dir to B $R_L = 250\Omega$ on the B/Y side t_P load				50	ns
tp_{ZH}			Fig 1.			30	
tp_{LZ}						50	
tp_{ZL}						30	
tp_{HZ}	Output enable/ disable time	Dir to A $R_L = 250\Omega$	1			15	ns
tp_{ZH}			Fig 1.			50	
tp_{LZ}						15	
tp_{ZL}						50	
tp_{HZ}	Output enable/ disable time	$\overline{OEA}$ to A $R_L = 250\Omega$	3			6	ns
tp_{ZH}			Fig 1.			12	
tp_{LZ}						6	
tp_{ZL}						12	

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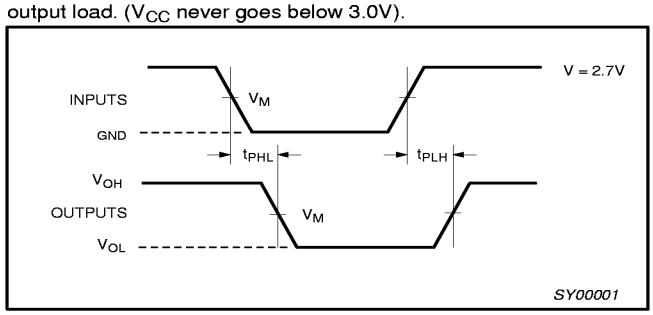
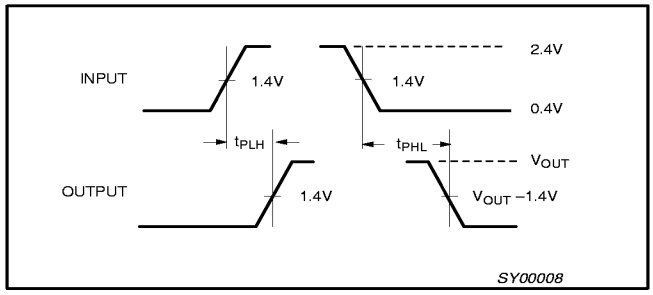
AC WAVEFORMS

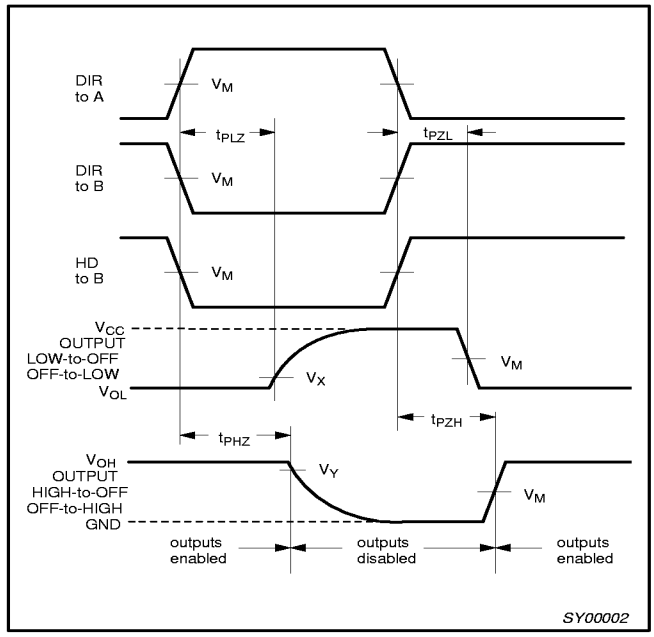
V_M = 1.5V
$V_X = V_{OL} \pm 0.3V$
$V_Y = V_{OH} - 0.3V$
V_{OL} and V_{OH} are the typical output voltage drops that occur with the output load. (V_{CC} never goes below 3.0V).



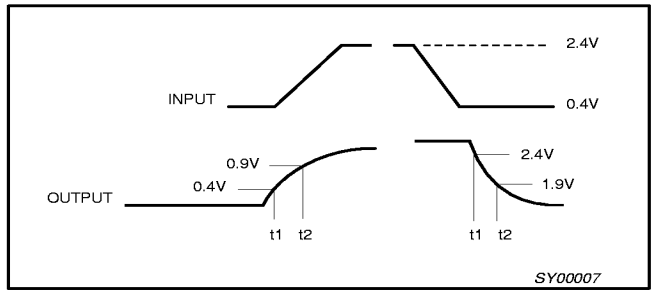
Waveform 1. Input Bn to output An propagation delays



Waveform 2. Voltage Waveforms Propagation Delay Times (A To B) Measured at Output Pin



Waveform 3. 3-State enable and disable times



Waveform 4. Slew Rate Voltage Waveforms on B/Y side
(Input pulse rise and fall time are 3ns, 150ns < pulse width < 10 µs, for both a Low to High and a High to Low transition.)
Slew Rate measured between 0.4V and 0.9V - rising.
Slew Rate measured between 2.4V and 1.9V - falling.
Slew Rate measured at V_{OUT} as specified in Waveform 5.

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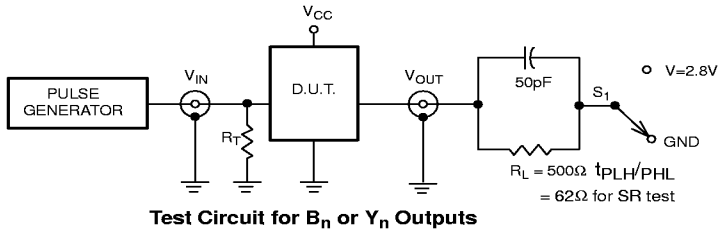
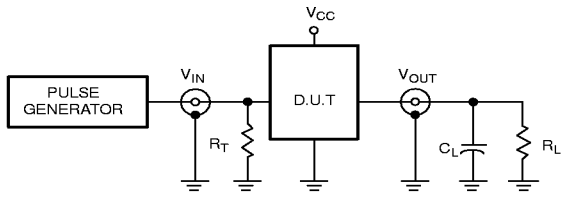
TEST CIRCUITS AND WAVEFORMS



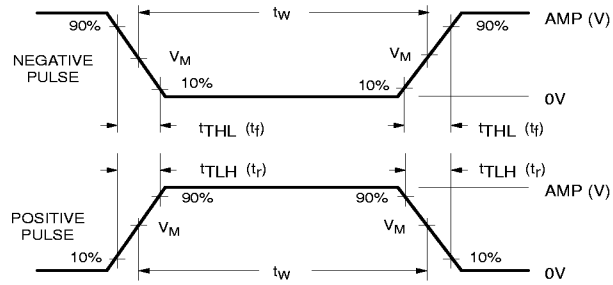
Test Circuit for B_n or Y_n Outputs

SWITCH POSITION
Bn or Yn Outputs

TEST	SWITCH
t_{PLH} t_{PHL}	GND V=2.8V



Test Circuit for A_n Outputs



V_M = 1.5V
Input Pulse Definition

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

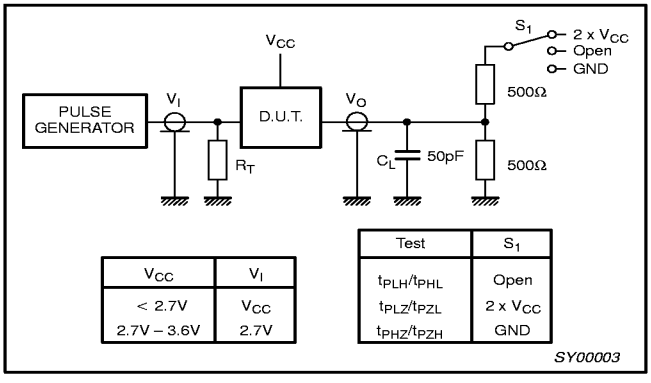
R_L = Load resistor; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_r	t_f
PDI1284	3.0V	1MHz	500ns	3ns	3ns

SV001741

Waveform 5.

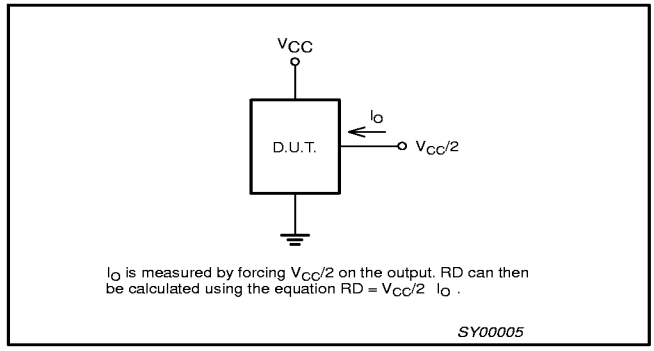


V_{CC}	V_I
< 2.7V	V_{CC}
2.7V – 3.6V	2.7V

Test	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 x V_{CC}
t_{PHZ}/t_{PZH}	GND

SY00003

Figure 1. Load Circuitry for Bn to An Switching Times



SY00005

Figure 2. Output Impedance RD

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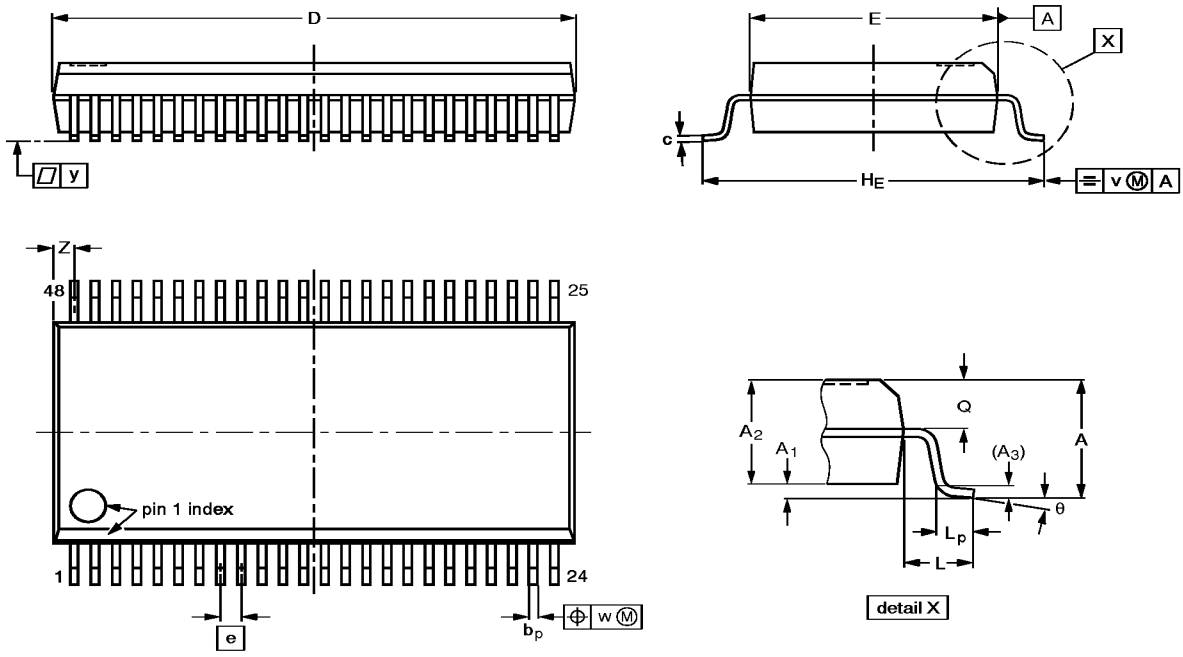
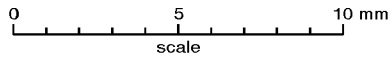
SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

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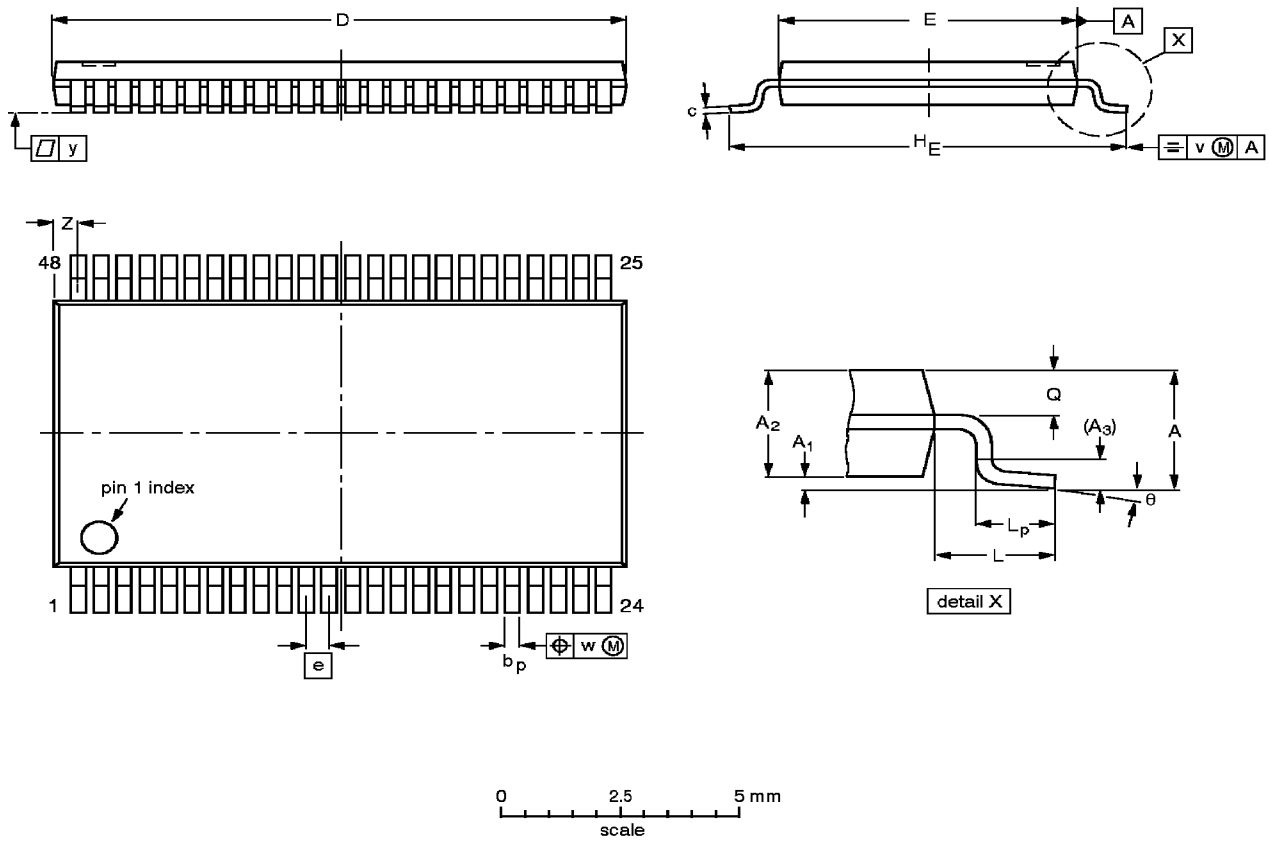
TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

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